Patent
Attorney's Docket No. 031941-092

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Per LIGANDER et al.	Group Art Unit: Unassigned
Application No.: Unassigned	Examiner: Unassigned
Filed: August 30, 2001	
For: Sequentially Processed Circuitry	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Before examination, please amend this application as follows

IN THE SPECIFICATION

Page 1, line 1, please **DELETE** "E42 P 39 US SBP";

line 2, please **DELETE** "2001-08-28";

line 7, please **REPLACE** the section heading with --Background--; and

line 10, **DELETE** the section heading entirely.

Page 6, please **REPLACE** the paragraph beginning at line 14, with the following:

--Encapsulation of printed circuits, with or without active and/or passive circuitry, that are processed sequentially is necessary to prevent destruction of the circuit patterns, especially if they are made of environmentally sensitive materials and/or with very thin layers. There is a desire to reduce conductors of a circuit board to less than 5 μm thick and less than 20 μm wide. This has raised an interest in using less stable polymers such as acrylat as thin layers of dielectric. It has been proposed to use offset printing for manufacturing printed circuit boards and also for manufacture of active and passive components, such as transistor functions,

resistors, capacitors, sensors, and emitters, with the same process by means of arranging tracks of conductive and semi conductive polymers. The process used is of an additive type. Using offset printing technology will enable manufacturing of surfaces in the order of 450 mm by 600 mm for a multiple of products with sizes in the range of approximately 100 mm by 150 mm to 10 mm by 10 mm. The finished products are unfortunately extremely sensitive to external physical contact. According to the invention, sequentially processed layers are built on an interface carrier. Thereafter a layer of adhesive is added to cover the sequentially processed layers and then a support carrier is stuck onto the adhesive. Alternatively a layer of adhesive is added to a support carrier after which the interface carrier is stuck to the support carrier with the sequentially processed layers closest to the adhesive on the support carrier. A sandwich construction is thus attained with the interface carrier on one side and the support carrier on the other side protecting the fragile layers within.--

Page 7, please **REPLACE** the paragraph beginning at line 6, with the following:

--As an example, a temperature log of frozen merchandize is desired. An appropriate circuit layout is manufactured on an interface carrier of at least semi-transparent polyester. The circuit side is joined by an adhesive with a cardboard box in which the frozen merchandize is to be transported. The cardboard box of the frozen merchanize will then function as the support carrier. The circuit with appropriate arranged tracks as sensors is mounted directly onto the object to be monitored and a readout of conditions can be made through the interface carrier by means of appropriate tracks arranged as light emitting diodes. The adhesive layer between the cardboard box, the support carrier, and the circuit can be shaped such that sensors or electrical contacts are not covered but have a direct contact with the support carrier, while at the same time providing a sufficient seal.--

Page 9, please **REPLACE** the paragraph beginning at line 13 with the following:

--In a final step, as shown in Figure 1e, a support carrier 199 is stuck onto the adhesive layer 190. Or alternatively a carrier with an adhesive layer is stuck onto the sequentially processed layers. The support carrier 199 will typically be in the order of millimeters to approximately 200 μm thick. The main purpose of the support carrier 199 is to provide a physical barrier and protection to the sensitive sequentially processed layers 110, 120. The support carrier 199 can, for example, be of paper, plastic or metal, be bendable or rigid, be a part of a chassis or cover/case/housing of an apparatus in which the circuit board arrangement is mounted, or be a carrier/box onto which the circuit board arrangement is mounted. As an example, the casing might be of a mobile phone or an accessory to it, such as a BlueTooth™ accessory, in which case the total electronic circuitry, with or without active or passive components, will take very little space and still be very well protected. If the support carrier 199 is a part of a casing, then most likely it will not be plane. The support carrier 190 may also comprise apertures, then preferably aligned with any apertures in the adhesive layer 190, for electrical access or access to any sensor on the outermost sequentially processed layer 120.--

Please **REPLACE** the Abstract with the following:

--An encapsulated circuit board arrangement including a thin interface layer with one or more vias for input/output interface to the circuit is presented. The encapsulated circuit board arrangement further includes one or more sequentially processed layers added to one side of the interface circuit. The sequentially processed layers are preferably made by additive offset printing technology. The encapsulated circuit board arrangement further includes a layer of adhesive. A first side of the adhesive layer is attached on top of the uppermost and most exposed layer. The encapsulated circuit board arrangement further includes a support carrier attached on a second side of the adhesive layer.--

IN THE CLAIMS

Please **CANCEL** claims 1-36.

Please **ADD** new claims 37-72 as follows:

37. A process of forming an encapsulated circuit board arrangement having at least one layer of tracks, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, the process comprising the steps of:

applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

38. The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer on top of the last applied sequentially processed layer.

39. The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer to the support carrier.

40. The process according to claim 37, wherein at least one of the at least one sequentially processed layer is applied using offset printing technology.

41. The process according to claim 40, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying an

acrylate as a dielectric of at least one of the at least one sequentially processed layer.

42. The process according to claim 38, wherein the adhesive layer is applied using offset printing technology.

43. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of a cover housing in which the encapsulated circuit board arrangement is mounted.

44. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

45. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is rigid.

46. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is bendable.

47. The process according to claim 37, wherein the step of applying at

least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having connection circuitry.

48. The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one passive component.

49. The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one active component.

50. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one via.

51. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one solid via.

52. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is bendable.

53. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is made of polymide.

54. A wireless communication device, comprising:
an encapsulated circuit board arrangement manufactured by applying at least

one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

55. A wireless mobile terminal, comprising:

an encapsulated circuit board arrangement manufactured by applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

56. An encapsulated circuit board arrangement having at least one sequentially processed track layer, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, wherein the circuit board arrangement comprises:

an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.

57. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer is applied using offset printing technology.

58. The circuit board arrangement according to claim 56, wherein a dielectric of at least one of the at least one sequentially processed layer is acrylate.

59. The circuit board arrangement according to claim 56, wherein the adhesive layer is applied using offset printing technology.

60. The circuit board arrangement according to claim 56, wherein the support carrier is at least a part of a cover housing in which the encapsulated circuit is mounted.

61. The circuit board arrangement according to claim 56, wherein the support carrier is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

62. The circuit board arrangement according to claim 56, wherein the support carrier is rigid.

63. The circuit board arrangement according to claim 56, wherein the support carrier is bendable.

64. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes connection circuitry.

65. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes tracks arranged as at

least one passive component.

66. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes tracks arranged as at least one active component.

67. The circuit board arrangement according to claim 56, wherein the interface layer includes at least one via.

68. The circuit board arrangement according to claim 67, wherein at least one of the at least one via is solid.

69. The circuit board arrangement according to claim 56, wherein the interface carrier is bondable.

70. The circuit board arrangement according to claim 56, wherein the interface carrier includes polymide.

71. A wireless communication device, comprising:

an encapsulated circuit board arrangement having an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.

72. A wireless mobile terminal, comprising:

an encapsulated circuit board arrangement having an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.

REMARKS

The specification and Abstract have been amended and the claims have been replaced to place the application in better form for examination. Favorable consideration is respectfully solicited.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: ______________________
Stephen J. Tytran
Registration No. 45,846

P.O. Box 1404
Alexandria, Virginia 22313-1404
(919) 941-9240

Date: August 30, 2001

"Express Mail" mailing label No EL766105323

Date of Deposit 08/30/01

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1 10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

J Snead
(Type or printed name of person mailing paper or fee)

____
(Signature of person mailing paper or fee)

Attachment to Preliminary Amendment dated August 30, 2001

Marked Up Copy of Amendments
to the Specification Section Headings

Section heading at page 1, line 7, delete "Technical Field" and insert therefor --Background--.

Section heading at page 1, line 10, delete entirely.

Paragraph beginning at page 6, line 14:

Encapsulation of printed circuits, with or without active and/or passive [cuircuitry] circuitry, that are processed sequentially is necessary to prevent destruction of the circuit patterns, especially if they are made of environmentally sensitive materials and/or with very thin layers. There is a desire to reduce conductors of a circuit board to less than 5 μm thick and less than 20 μm wide. This has raised an interest in using less stable polymers such as acrylat as thin layers of dielectric. It has been proposed to use offset printing for manufacturing printed circuit boards and also for manufacture of active and passive components, such as transistor functions, resistors, capacitors, sensors, and emitters, with the same process by means of arranging tracks of conductive and semi conductive polymers. The process used is of an additive type. Using offset printing technology will enable manufacturing of surfaces in the order of 450 mm by 600 mm for a multiple of products with sizes in the range of approximately 100 mm by 150 mm to 10 mm by 10 mm. The finished products are unfortunately extremely [sensitve] sensitive to external physical contact. According to the invention, sequentially processed layers are built on an interface carrier. Thereafter a layer of adhesive is added to cover the sequentially processed layers and then a support carrier is stuck onto the adhesive. Alternatively a layer of adhesive is added to a support carrier after which the interface carrier is stuck to the support carrier with the sequentially processed layers closest to the adhesive on the support carrier. A sandwich construction is thus attained with the interface carrier on one side and the support carrier on the other side protecting the fragile layers within.

Paragraph beginning at page 6, line 6:

As an example, a temperature log of [a] frozen merchandize is desired. An appropriate circuit layout is manufactured on an interface carrier of at least semi-transparent polyester. The circuit side is joined by an adhesive with a cardboard box in which the frozen merchandize is to be transported. The cardboard box of the frozen merchanize will then function as the support carrier. The circuit with appropriate arranged tracks as sensors is mounted directly onto the object to be monitored and a readout of conditions can be made through the interface carrier by means of appropriate tracks arranged as light emitting diodes. The adhesive layer between the [carboard] cardboard box, the support carrier, and the circuit can be shaped such that sensors or electrical contacts are not covered but have a direct contact with the support carrier, while at the same time providing a sufficient seal.

Paragraph beginning at page 9, line 13:

In a final step, as shown in Figure 1e, a support carrier 199 is stuck onto the adhesive layer 190. Or alternatively a carrier with an adhesive layer is stuck onto the sequentially processed layers. The support carrier 199 will typically be in the order of millimeters to approximately 200 μm thick. The main purpose of the support carrier 199 is to provide a physical barrier and protection to the sensitive sequentially processed layers 110, 120. The support carrier 199 can, for example, be of paper, plastic or metal, be bendable or rigid, be a part of a [chassi] chassis or cover/case/housing of an apparatus in which the circuit board arrangement is mounted, or be a carrier/box onto which the circuit board arrangement is mounted. As an example, the casing might be of a [mobil] mobile phone or an accessory to it, such as a [blue tooth] BlueTooth™ accessory, in which case the total electronic circuitry, with or without active or passive components, will take very little space and still be very well protected. If the support carrier 199 is a part of a casing, then most likely it will not be plane. The support carrier 190 may also comprise apertures, then preferably aligned with any apertures in the adhesive layer 190, for electrical access or access to any sensor on the outermost sequentially processed layer 120.

Attachment to Preliminary Amendment dated August 30, 2001

Marked Up Copy of Amendments
to the Abstract

An encapsulated circuit board arrangement [comprising] including a thin interface layer with one or more vias for input/output interface to the circuit is presented. The encapsulated circuit board arrangement further [comprises] includes one or more sequentially processed layers added to one side of the interface circuit. The sequentially processed layers are preferably made by additive offset printing technology. The encapsulated circuit board arrangement further [comprises] includes a layer of adhesive. A first side of the adhesive layer is attached on top of the uppermost and most exposed layer. The encapsulated circuit board arrangement further [comprises] includes a support carrier attached on a second side of the adhesive layer.